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EXAMINER	
SINGH, HIRDEPAL	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/709,022	HSIAO, YUAN-KUN	
	Examiner	Art Unit	
	HIRDEPAL SINGH	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 March 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,9-14 and 16-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-7,9,10,12-14,16,17,19-23,25 and 26* is/are rejected.

7)☒ Claim(s) *4, 11, 18 and 24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This action is in response to the amendment filed on March 03, 2008. Claims 21-26 are added, now claims 1-7, 9-14 and 16-26 are pending and have been considered below.

Response to Arguments

2. The amendment has corrected the informality in claim 7. Therefore, the objection is withdrawn.

3. Applicant's arguments filed March 03, 2008 have been fully considered but they are not persuasive.

Applicant argues "…none of Hsu, Takumai, and Banno disclose a decision logic circuit.., for generating a third counting value based on the first counting value and the second counting value ...." and "…nothing in the description of the phase detection circuit or Hsu in general teaches or suggests generating a third counting value or calculating a sum of a plurality of the third counting values…Takumai and Banno fail to disclose generating a third counting value and calculating a sum …The cited references also fail to disclose setting the phase adjusting value to zero if the sum is within a specified range, and setting the phase adjusting value according to the sum if the sum is outside the specified range…There is no further decision logic for determining whether to generate a phase adjustment signal."

4. Examiner respectfully traverse applicant's opinion as the Prior art of record Hsu et al disclose a phase adjusting circuit with all the limitations are disclosed in the

combination. To facilitate the understanding of rejection based on Hsu, Takumai, and Banno and an explanation of the arguments is as follows: Hsu discloses the phase detection circuit as in figure 6, detect the phase shift or phase difference between the target clock and the wobble clock and accordingly adjust the phase adjusting circuit by sending a control signal even in the case the phase shift in out of locking range (column 7, lines 8-16 and 32-42); and Takumai discloses to adjust the phase when the phase of ATIP synchronization signal leads phase of data synchronization signal the phase of ATIP synchronization signal is advance and vice versa (clearly shown in figures 9 and 11); and Banno discloses the phase comparing circuit compares the phase of ASYNC signal and ESFS signal and accordingly generate up count and down count signal in the counters the number of pulses i.e. counter value determines the phase adjusting value or the phase difference which is used to adjust the phase (figure 4; paragraph 0099). Therefore, in combination the cited reference teaches the counter values in the up and down counter in Banno to determine phase adjusting value based on phase difference in the counted pulses, in combination with internal counter (271 figure 1) of Takumai generates equivalent third counting value also determine if phase of ATIP synchronization signal leads phase of data synchronization signal to advance or delay the phase, and the Hsu phase shift detection and adjusting circuit adjust i.e. advance or delay the phase even if the phase shift in outside the specified range.

5. From the above discussion it is clear that the combination of cited prior art has all the claimed limitations. Therefore, the rejection is upheld.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1, 7, 13-14, 20-21 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu et al. (US 6,754,147) in view of Takumai et al. (US 2003/0081516) and further in view of Banno (US 2004/0057360).

Regarding claim 1:

Hsu et al discloses a phase adjusting circuit (figure 6) for generating a phase adjusting value based on the phase difference of a target clock signal and an input signal, the phase adjusting circuit comprising:

a phase-frequency detector (12 in figure 6) for generating a first control signal and a second control signal by comparing the phase of the input signal with the phase of the target clock signal;

a decision logic circuit (104 and 106 in figure 6) connected to the counter for generating a third counting value based on the first counting value and the second counting value, calculating the sum of a plurality of the third counting values setting the phase adjusting value to zero if the sum is within a specified range, and setting the phase adjusting value according to the sum if the sum is outside the specified range

(column 7, lines 8-16 and 32-42, adjusting the phase even if outside range , and inherently no adjustment or correction required if phases are synchronized).

Hsu et al discloses all of the subject matter as described above except for specifically teaching (1) a clock generator for generating a reference clock; (2) a counter connected to the phase-frequency detector and the counter for generating a first counting value by counting the number of cycles of the reference clock during the duration of the first control signal, and generating a second counting value by counting the number of cycles of the reference clock during the duration of the second control signal.

However, regarding item (1) above, Takumai et al in the same field of endeavor discloses a system for adjusting the phase of the clock comprising a clock generator (system clock; paragraph 0075) for generating a reference clock; and regarding item (2) above, a counter (271 in figures 1 and 15) connected to the phase-frequency detector (270 which is further connected to 243 in figure 15).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to combine a counter between the phase frequency detector and control logic to count the number of pulses of the system clock signal as suggested by Takumai in Hsu system in order to get the information related to the phase difference of the incoming signal and the target clock signal so that the counter starts counting based on the control signal i.e. whether the input signal leads or lags the target clock signal, in this way the target clock is easily adjusted and controlled according to the input signal

also whenever there is a phase difference between input and target clock the phase adjustment circuit makes the adjustment quickly.

Also, regarding item (2) above, Banno in the same field of endeavor discloses a system for adjusting the phase of incoming clock signal where a counter (142-143 in figure 4 “this is obvious and well known that an up/down counter does the same function as an up and a down counter and can be used interchangeably ”) connected to the phase-frequency detector (141 in figure 4) and the counter for generating a first counting value by counting the number of cycles of the reference clock during the duration of the first control signal (paragraph 0097), and generating a second counting value by counting the number of cycles of the reference clock during the duration of the second control signal (paragraph 0099).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to combine the counter as used in Banno to count the number of pulses of the clock signal in Hsu system in order to get the information related to the phase difference of the incoming signal and the target clock signal so that the counter starts counting based on the control signal i.e. whether the input signal leads or lags the target clock signal, in this way the target clock is easily adjusted and controlled according to the input signal also whenever there is a phase difference between input and target clock the phase adjustment circuit makes the adjustment quickly.

Regarding claims 7, 14 and 21:

Hsu et al discloses a clock signal adjusting circuit comprising:

a phase adjusting circuit (108 in figure 6) for generating a phase adjusting value based on an input signal and a target clock signal, the phase adjusting circuit comprising:

a phase-frequency detector (12 in figure 6) for generating a first control signal and a second control signal by comparing the phase of the input signal with the phase of the target clock signal;

a decision logic circuit (104 and 106 in figure 6) connected to the counter for generating a third counting value based on the first counting value and the second counting value, calculating the sum of a plurality of the third counting values and comparing the sum with a predetermined range for outputting the phase adjusting value as the counting times are increased to equal to a predetermined (as clearly stated in claim 1 last limitation) counting times.

Hsu et al discloses all of the subject matter as described above except for specifically teaching that (1) a clock generator for generating a reference clock; (2) a counter connected to the phase-frequency detector and the counter for generating a first counting value by counting the number of cycles of the reference clock during the duration of the first control signal, and generating a second counting value by counting the number of cycles of the reference clock during the duration of the second control signal; (3) a frequency divider connected to the phase adjusting circuit for adjusting the target clock signal by dividing the frequency of a first reference clock based on the phase adjusting value.

However, regarding item (1) above, Takumai et al in the same field of endeavor discloses a system for adjusting the phase of the clock comprising a clock generator (system clock; paragraph 0075) for generating a reference clock; and regarding item (2) above, a counter (271 in figures 1 and 15) connected to the phase-frequency detector (270 which is further connected to 243 in figure 15).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to combine a counter between the phase frequency detector and control logic to count the number of pulses of the system clock signal as suggested by Takumai in Hsu system in order to get the information related to the phase difference of the incoming signal and the target clock signal so that the counter starts counting based on the control signal i.e. whether the input signal leads or lags the target clock signal, in this way the target clock is easily adjusted and controlled according to the input signal also whenever there is a phase difference between input and target clock the phase adjustment circuit makes the adjustment quickly.

Also, regarding item (2) above, Banno in the same field of endeavor discloses a system for adjusting the phase of incoming clock signal where a counter (142-143 in figure 4 “this is obvious and well known that an up/down counter does the same function as an up and a down counter and can be used interchangeably ”) connected to the phase-frequency detector (141 in figure 4) and the counter for generating a first counting value by counting the number of cycles of the reference clock during the duration of the first control signal (paragraph 0097), and generating a second counting

value by counting the number of cycles of the reference clock during the duration of the second control signal (paragraph 0099).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to combine the counter as used in Banno to count the number of pulses of the clock signal in Hsu system in order to get the information related to the phase difference of the incoming signal and the target clock signal so that the counter starts counting based on the control signal i.e. whether the input signal leads or lags the target clock signal, in this way the target clock is easily adjusted and controlled according to the input signal also whenever there is a phase difference between input and target clock the phase adjustment circuit makes the adjustment quickly.

Regarding item (3) above, Takumai et al in the same field of endeavor discloses a system for adjusting the phase of the clock signal where a frequency divider (242 in figures 1 and 15) connected to the phase adjusting circuit for adjusting the target clock signal by dividing the frequency of a first reference clock based on the phase adjusting value.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to use a frequency divider as suggested by Takumai in Hsu system in order to make the phase and frequency of the incoming clock signal in accordance with the adjustment value to make the system clock correct which is advantageous as the clock is adjusted according to the wobble signal and the frequency divider and the delay value in combination make sure the correct clock signal.

Regarding claims 13, 20 and 26:

Hsu et al discloses all of the subject matter as described above and further discloses that the system is applicable in an optical disc drive (title) where the input signal being a wobble signal of an optical disc, the target clock signal being a corresponding wobble clock (figure 6) generated by the optical disc drive based on the wobble signal.

8. Claims 2-3, 5, 9-10, 16-17 and 22-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu et al. (US 6,754,147) in view of Takumai et al. (US 2003/0081516) further in view of Banno (US 2004/0057360) as applied to claims 1, 7, 14 and 21 above and further in view of Von Kaenel (US 2003/0067335).

Regarding claims 2 and 3:

Hsu et al discloses all of the subject matter as described above except for specifically teaching the first control signal is generated when the phase of the input signal leads the phase of the target clock signal and the second control signal is generated when the phase of the input signal lags the phase of the target clock signal.

However, Von Kaenel in the same field of endeavor discloses a system for adjusting the phase of the clock where the first control signal is generated when the phase of the input signal leads the phase of the target clock signal (paragraph 0018, lines 12-14) the second control signal is generated when the phase of the input signal lags the phase of the target clock signal (paragraph 0018, lines 14-16). Also Takumai et al in the same field of endeavor discloses the first control signal is generated when the phase of the input signal leads the phase of the target clock signal (paragraph 0071).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to use a counter in Hsu system in order to get the information related to the phase difference of the incoming signal and the target clock signal so that the counter starts counting based on the control signal i.e. whether the input signal leads or lags the target clock signal, in this way the target clock is easily adjusted and controlled according to the input signal also whenever there is a phase difference between input and target clock the phase adjustment circuit makes the adjustment quickly.

Regarding claim 5:

Hsu et al discloses all of the subject matter as described above except for specifically teaching that the first counting value is a positive value, the second counting value is a negative value, and the third counting value is the sum of the first counting value and the second counting value.

However, Takumai et al in the same field of endeavor discloses a system for adjusting the phase of the clock signal where a counter (271 in figures 1 and 15) counts a first positive counting value (paragraph 0075; figure 6).

Also Von Kaenel in the same field of endeavor discloses a system for adjusting clock signal where counter (14 in figure 1) counts a first positive counting value, the second counting value is a negative value (paragraphs 0017, 0025 and 0035; the up counting value is positive and down counting value is negative), and the third counting value is the sum of the first counting value and the second counting value.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to implement a counter as taught by Takumai to control the phase of

the incoming signal by adjusting the gain to change the frequency division ratio to further compensate for the phase and using the up/down or positive negative values of the Von Kaenel counter to control the phase (generate a decision or third value based on the up/down or positive negative values of the counter) of the incoming signal in Hsu system to make quick adjustment to the clock signal.

Regarding claims 9, 10, 16, 17, 22 and 23:

Hsu et al discloses all of the subject matter as described above except for specifically teaching the first control signal is generated when the phase of the input signal leads the phase of the target clock signal and the second control signal is generated when the phase of the input signal lags the phase of the target clock signal.

However, Von Kaenel in the same field of endeavor discloses a system for adjusting the phase of the clock where the first control signal is generated when the phase of the input signal leads the phase of the target clock signal (paragraph 0018, lines 12-14) the second control signal is generated when the phase of the input signal lags the phase of the target clock signal (paragraph 0018, lines 14-16). Also Takumai et al in the same field of endeavor discloses the first control signal is generated when the phase of the input signal leads the phase of the target clock signal (paragraph 0071).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to use a counter in Hsu system in order to get the information related to the phase difference of the incoming signal and the target clock signal so that the counter starts counting based on the control signal i.e. whether the input signal leads or lags the target clock signal, in this way the target clock is easily adjusted and controlled

according to the input signal also whenever there is a phase difference between input and target clock the phase adjustment circuit makes the adjustment quickly.

9. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu et al. (US 6,754,147) in view of Takumai et al. (US 2003/0081516) further in view of Banno (US 2004/0057360) as applied to claim 1 above, and further in view of Fukuhara (US 2002/0027966).

Regarding claim 6:

Hsu et al discloses all of the subject matter as described above except for specifically teaching that the phase-frequency detector is further able to receive a protection signal to stop outputting the phase adjusting value for avoiding interference generated from an unstable input signal.

However, Fukuhara in the same field of endeavor discloses a system for adjusting the phase of the clock signal where a phase-frequency detector is further able to receive a protection signal (paragraphs 0008 and 0065) to stop outputting the phase adjusting value for avoiding interference generated from an unstable input signal.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to use a protection signal in the phase adjusting circuit in order to stop it for sending phase adjustment signal to avoid an error occurred in the incoming wobble signal by the signal processing done on the modulated part of the signal i.e. the address containing part of the wobble signal is modulated and it could give an error signal which if used to adjust the clock of the wobble signal could cause the wrongly adjusted clock

as the phase adjustment is influenced by the error generated in the wobble signal, the protection signal is able to avoid generating the wrong clock and makes the circuit work properly.

10. Claims 12, 19 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu et al. (US 6,754,147) in view of Takumai et al. (US 2003/0081516) further in view of Banno (US 2004/0057360) as applied to claims 7 and 14 above, and further in view of Nakao et al. (US 5,939,947).

Regarding claims 12, 19 and 25:

Hsu et al discloses all of the subject matter as described above except for specifically teaching that the frequency divider comprises:

a counter for counting the cycle number of cycles of the first reference clock and resetting the cycle number after each predetermined number of cycles of the first reference clock; a register for storing the phase adjusting value; a comparator connected to the counter and the register for generating an enable signal when the cycle number of the first reference clock is equal to the phase adjusting value; a pulse generator connected to the comparator for generating an impulse when receiving the enable signal; a flip-flop having a trigger input terminal connected to the pulse generator for outputting the target clock signal while receiving the impulse; and an inverter having an input terminal for receiving the target clock signal and inverting the target clock signal to feedback to the input of the flip-flop.

However, Nakao et al in the same field of endeavor discloses that the frequency divider comprises a counter (38b in figures 1 and 3) for counting the cycle number of cycles of the first reference clock and resetting the cycle number after each predetermined number of cycles of the first reference clock; a register (40 in figures 1 and 3) for storing the phase adjusting value; a comparator (3b in figures 1 and 3) connected to the counter and the register for generating an enable signal when the cycle number of the first reference clock is equal to the phase adjusting value; a pulse generator connected to the comparator for generating an impulse when receiving the enable signal (column 3 lines 60-66); a flip-flop (39 in figures 1 and 3) having a trigger input terminal connected to the pulse generator for outputting the target clock signal while receiving the impulse; and an inverter having an input terminal for receiving the target clock signal and inverting the target clock signal to feedback to the input of the flip-flop (column 4, lines 1-10).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to use a frequency dividing circuit comprising a counter, register, comparator, pulse generation means, flip flop and feeding back the inverted output of flip flop as the advantage of using a frequency dividing circuit comprising these components is to get the clock signal which is true wobble clock signal.

Allowable Subject Matter

11. Claims 4, 11, 18 and 24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

12. The following is a statement of reasons for the indication of allowable subject matter: The prior art of record Hsu et al discloses a phase adjusting circuit that adjust the phase based on control signal depending on the phase shift value in a counter, but fails to disclose the frequency of the reference clock signal is N times the frequency of target clock and adjusting the phase based on control signal that is generated according to a specified range, which ranges from a positive number of N/2 to a negative number having absolute value of N/2.

Conclusion

13. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to HIRDEPAL SINGH whose telephone number is (571)270-1688. The examiner can normally be reached on Mon-Fri (Alternate Friday Off)8:00AM-5:00PMEST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Shuwang Liu can be reached on 571-272-3036. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/H. S./
Examiner, Art Unit 2611
/Shuwang Liu/
Supervisory Patent Examiner, Art Unit 2611